LOW PHASE NOISE, FULLY INTEGRATED MONOLITHIC VCO IN X BAND BASED ON HBT TECHNOLOGY

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***Abstract* — This paper presents a very low phase noise wide band fully integrated VCO in X band. It is based on UMS HBT technology (HB20P process). This circuit has been realized in the frame of ARGOS project in order to carry out a low phase noise frequency synthesizer. HB20P transistor and varactor nonlinear models have been extracted from pulsed measurements. Furthermore, HBT low frequency noise measurements have been performed to evaluate noise sources and then to optimize the operating point in the design. According to these characterizations, we have realized a fully MMIC VCO providing good phase noise performances (-90 dBc/Hz @ 100 KHz), in a wide frequency band (15 %) and in a wide temperature range (-40°C < T < +65°C).**

I. INTRODUCTION

Recent years have shown real advances of microwave monolithic integrated circuit (MMIC) for low cost millimeter-wave systems, such as wireless communication and automotive radar systems [1]. The oscillator is the critical circuit in mm-wave front-end, which has to be optimized in terms of:

- Phase noise performance
- Center frequency control flexibility
- Low cost manufacturing
- Chip size reduction

Today, GaAs HBT exhibits interesting characteristics, such as high gain and low frequency noise performances allowing to reach low phase noise for fully monolithic integrated VCOs. An X-band VCO has been fabricated with UMS HBT technology (HB20P process) in the frame of ARGOS project in order to realize a low phase noise frequency synthesizer.

Firstly, the low frequency noise characterization of the transistor at different biasing conditions is presented. Secondly, the nonlinear modeling procedure of transistor and varactor will be described : from I(V) and multi-bias S parameter measures, up to nonlinear model. In a third part, the design procedure will be developed. Based on the previous noise measures, the nonlinear model and an efficient topology, a good compromise has been reached between low phase noise and output power, by limiting the load cycle of the transistor in areas where noise sources are low. The X band fully integrated VCO-chips developed and tested by UMS, have been validated for the following characteristics:

- Frequency band & output power at ambient temperature (Tamb = 25°C)
- Phase noise versus the tuning voltage at Tamb
- Phase noise & Frequency band versus temperature (-40°C<T<+65°C).

II. LOW FREQUENCY NOISE MEASUREMENTS

The aim of these investigations was to identify the major low frequency (LF) noise sources in the active devices, and to measure the variation of their respective levels versus the bias conditions in order to improve the design rules of the VCO.

The first step has been a systematic measurement of the equivalent input noise sources in the operating zone of the transistor, the device dimensions featuring two emitter fingers of 2×30 µm. The equivalent input voltage and current noise spectral densities (S_V and S_I), and their correlation factor, have been measured using a multi-impedance technique [2]. The correlation factor is expressed in terms of a correlation resistance R_{cor}, which is compared to the sum of the base and emitter access resistances ($R_{bb'}+R_{ee'}$) previously extracted from the S parameter measurements.

In the case of the investigated device, R_{cor} has been found to be equal to $R_{bb'}+R_{ee'}$. This means that the equivalent noise source representation is, in this case, very close to the device physics. Moreover, the device noise modeling using a base emitter current noise source (which represents the noise in the active region) and base

and emitter contact voltage noise source (which accounts for noise at the ohmic contacts and in the extrinsic regions) is coherent with the small signal device modeling. We have therefore represented the dependence of S_V and S_I on the DC bias (I_{b0}, V_{ce0}) using 3D plots. An example is given in the Fig. 1 and 2, the LF noise data being those of the device at 10 kHz. A clear minimum is observed on the voltage noise at high V_{ce0} and medium I_{b0} bias. Concerning the current noise, it is almost independent of V_{ce0} and features a strong increase with I_{b0}.

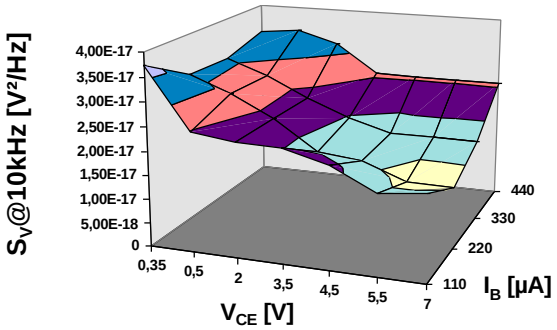

Fig. 1 Voltage spectral density at 10 Khz versus V_{ce} and I_b of the 2*30 µm HBT

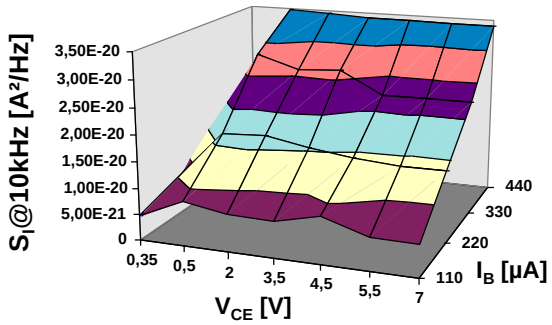

Fig. 2 Current spectral density at 10 Khz versus V_{ce} and I_b of the 2*30 µm HBT

III. Nonlinear Measures and Modelling

The characterization process relies on pulsed I-V and [S] parameters measurements [4]. Short pulses of typical duration of 500 ns are applied both on the base and the collector of the transistor with a repetition period of 6 µs, ensuring thus an isothermal characterization of the device. During the pulse duration, base and collector voltages and currents are measured simultaneously as well as the [S] parameters of the device in the 2 - 20 GHz frequency range. We acquire then the measurements necessary to obtain the electrical model. The I(V) and [S] parameters pulsed measurements have been performed for a bias point. The temperature of the device is fixed by the bias point, which allows isothermal measurements.

Fig. 3. presents the HBT model, with both transcapacitances Cbec and Cbce to take into consideration the Non-Quasi-Static (NQS) effects.

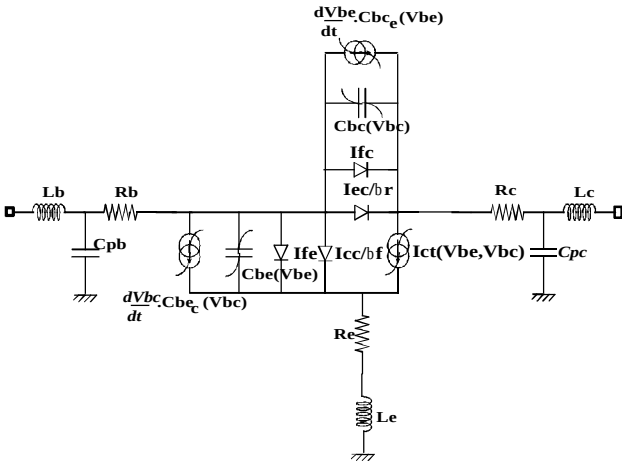

Fig. 3. : Non-linear NQS HBT model.

The expressions of all the non-linear elements are given in [5]. The comparison between measures and model of output Ic(Vce) characteristics, is shown in Fig. 4.

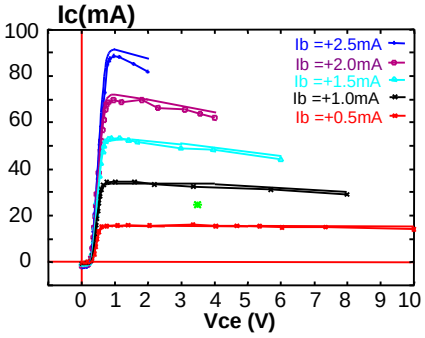

Fig. 3. : Comparison between measure and model

The values of model parameters are given in table I

Extrinsic elements	
Lb=33.83pH	Lc=27pH Le=20.71pH
Rb=4.22 Ω	Rc=1 Ω Re=1.55 Ω
Cpb=44 fF	Cpc=60 fF
ICT current source	
Ise = 3.4e-23	Ne = 1.096
Isc = 7.8e-29	Nc = 1.096
Beta_f = 43	Beta_r = 1

Leakage diodes
Isfe = 4.4e-16 Nfe = 1.97 Isfc = 3.0e-12 Nfc = 2.00
Capacity base-emitter
Cbej0 = 2.42e-13 ϕbe = 2 Cbe_d0=4.6e-2 Cbe_d1=18990 Nd=1.5 Cbe_c0 = 8e-17 Cbe_c1 = 5
Capacity base-collector
Cbcj0 = 1e-13 ϕbc = 2 Cbc_d0 = 8.4e-29 Cbc_e0 = 2.4e-2 Cbc_e1=18990 Nbc=1.096 Nbe=1.47
Constants
α = 0.95

Table II : Model parameters of HBT223

The models have been validated thanks to the comparison between measures of pulsed [S] parameters and computation ones, shown in Fig 5. The bias point is Vce = 3.5 V and Ic = 24 mA.

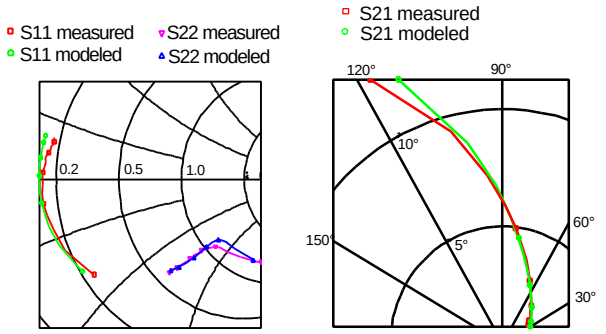

Fig. 5 : measured and simulated S parameters

IV. HBT MMIC VCO DESIGN FOR LOW PHASE NOISE

The following figure shows our proposed X band VCO topology using a transmittive structure between HBT base and collector.

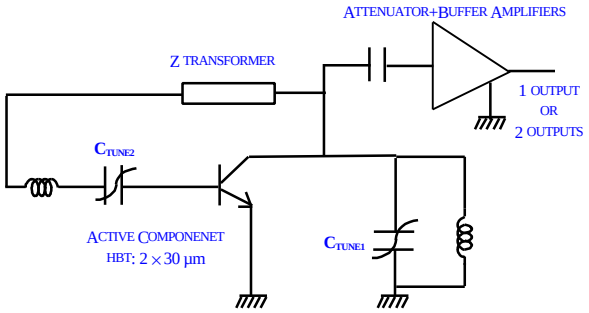

Fig. 6 : Simplified representation of the VCO topology

The three-terminal device (2 fingers × 30 µm of HBT emitter development) is used, as a fed-back amplifier circuit providing a sufficient open loop gain required for starting the oscillation at the specified frequency.

Our approach consists of using two varactors put in parallel and series configurations. The use of only one varactor (C_{TUNE1}) could be enough to obtain the required frequency band but margin is necessary for yield optimization. Indeed, the complete circuit has also been analyzed according to temperature and technology spreads. That explains the second varactor role, which can be considered for electronic tuning of center frequency control versus spreads and temperature, the main objective is to carry out a fully integrated VCO for a volume production. Furthermore, with C_{TUNE2}, we obtain an oscillator with a global higher Q and thus a lower phase noise.

The output circuit is composed of an attenuator followed by one or three buffer amplifiers in order to obtain one or two insulated outputs according to the specifications. The attenuator and buffer amplifiers contribute to reduce the pulling factor. In addition, buffer amplifiers provide a constant power in the frequency band (> 10 dBm) whatever the temperature.

The circuit analysis has been performed using standard microwave C.A.D. software by means of linear and nonlinear simulations.

The resulting optimized load cycle of the transistor is shown in Fig. 7:

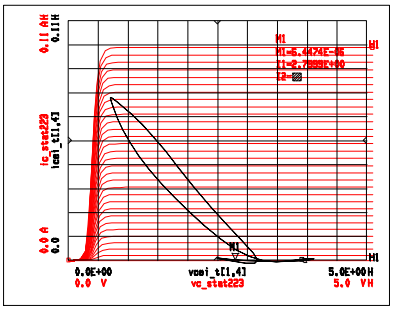

Fig.7 : transistor load cycle

It is a good compromise between output power and its excursion in areas where the noise sources are low (low I_b). The gain compression necessary to reach amplitude stabilization of the oscillation arises by the swing in the cut-off area of the transistor characteristics.

V – MEASUREMENT RESULTS

Chip tests have been performed using fixed DC voltage (+5V) applied to the chip and for 0 to 8 V tuning voltage range. Fig.7 shows measured oscillation frequency and output power versus tuning voltage. We can notice about 1.5 GHz frequency band and 13 dBm mean output power obtained with 2.3 mm^2 chip size. VCO phase noise performances are shown in fig.8 versus frequency offset from the carrier and for different tuning voltages. At 10 GHz and 100 kHz off-carrier, the measured phase noise is –92 dBc/Hz. These results have been validated at three different temperatures, between –40°C and 65°C (fig.9 and fig.10).

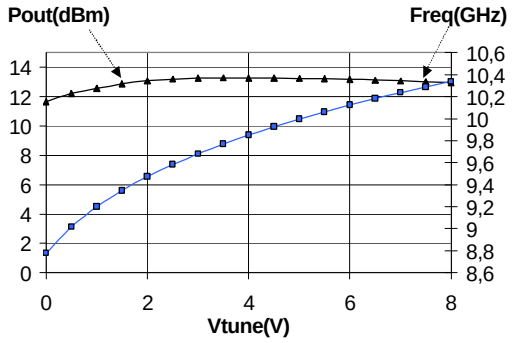

Fig. 7 : Frequency band and output power versus tuning voltage

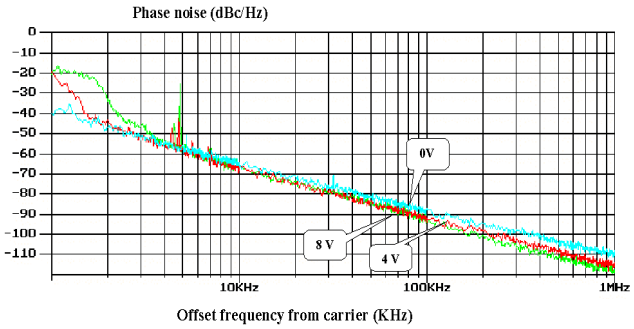

Fig. 8 : VCO phase noise @ Tamb versus frequency offset and tuning voltage

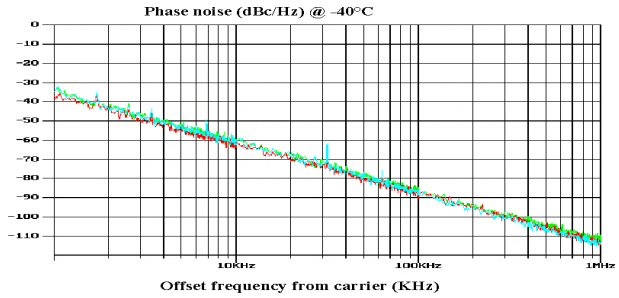

Fig. 9 : VCO phase noise @ -40°C versus frequency offset and tuning voltage

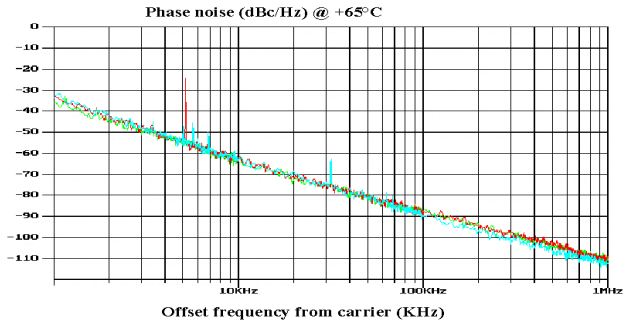

Fig. 10 : VCO phase noise @ +65°C versus frequency offset and tuning voltage

V. Conclusion

This paper presents the design and realization of a –90 dBc/Hz @ 100 KHz low phase noise VCO using UMS HBT20P process. This X band VCO, fully integrated exhibits a power greater than 11 dBm over the wide frequency band (15 %). Furthermore, the transistor and varactor used in the MMIC has been whole characterized. Low frequency noise sources measures and nonlinear measures and model, associated to an appropriate topology has allowed reaching this low phase noise.

Acknowledgement

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References

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